

WHAT IS CLAIMED IS:

1           1. A method for processing digital video signals for live video  
2 applications, the method comprising:  
3           providing video data comprising a plurality of frames;  
4           identifying a first frame and a second frame in the frame sequences;  
5           processing the information of the first frame and the information of the second  
6 frame to determine a quantization step value for the second frame;  
7           adjusting a transmission bit rate for the second frame in response to the  
8 quantization step value.

1           2. The method of claim 1 wherein the providing video data comprises:  
2           assigning compression modes to the frames.

1           3. The method of claim 2 wherein the compression modes are selected  
2 from a group comprising I-mode, P-mode, and B-mode.

1           4. The method of claim 1 wherein the processing the information of the  
2 first frame and the information of the second frame comprises:  
3           calculating a sigmaSAD value for the second frame;  
4           calculating a divisor value for the second frame;  
5           calculating the quantization step for the second frame.

1           5. The method of claim 4 wherein the calculating a sigmaSAD value  
2 comprises:  
3           calculating a SAD value for each microblock of the second frame;  
4           storing the SAD value in a memory unit for each microblock of the second  
5 frame;  
6           calculating the sum of all the SAD values for the second frame;  
7           dividing the sum by the total number of microblocks of the second frame.

1           6. The method of claim 4 wherein the calculating a divisor value  
2 comprises  
3           selecting a series of integers that is indexed from 0 through n-1;  
4           selecting a complexity integer;  
5           calculating the quotient modulo n of the complexity integer;

6 setting the divider value equal to an integer whose index in the series equals  
7 the quotient;

8 wherein n is an integer larger than 1.

1 7. The method of claim 6 wherein the selecting a complexity integer  
2 comprises:

3 if the second frame is an I-frame, setting the complexity integer near midrange  
4 between an integer A and an integer B;

5 if the second frame is not an I-frame, adjusting the complexity integer so that  
6 the fullness of a buffer varies toward a predefined fullness level.

1 8. The method of claim 4 wherein the calculating the quantization step  
2 comprises setting the quantization step equal to the sum of the ratio of the sigmaSAD value to  
3 the divisor value, and a constant.

9. The method of claim 8 wherein the constant equals 1.

10. The method of claim 1 wherein the processing the information of the  
first frame and the information of the second frame comprises:

deciding whether to encode a frame in the I-mode before any P-frame  
encoding is accomplished.

11. The method of claim 6 wherein the processing comprises:

Adjusting the complexity integer so that the size of encoded data for anyone of  
3 the plurality of frames has approximately an equal size.

12. The method of claim 1 wherein the method for processing digital video  
signals further comprises:

3 determining the locations of I-frames in the step of providing video data;  
4 extending frames immediately preceding the I-frames for one additional frame  
5 time;  
6 skipping frames immediately following the I-frames.

13. A system including a processor for processing digital video signals for  
2 live video applications, the system comprising:

3 a memory unit within which a computer program is stored, the computer  
4 program comprising:

5 code that instructs the processor to receive video data comprising a plurality of  
6 frames;  
7 code that directs the processor to identify a first frame and a second frame in  
8 the frame sequences;  
9 code that directs the processor to process the information of the first frame and  
10 the information of the second frame to determine a quantization step for the second frame.

1 14. The system of claim 13 wherein the code that directs the processor to  
2 process the information of the first frame and the information of the second frame comprises:  
3 code that calculates a sigmaSAD value for the second frame;  
4 code that calculates a divisor value for the second frame;  
code that calculates the quantization step for the second frame.

15. The code of claim 14 that calculates a sigmaSAD value comprises:  
code that calculates a SAD value for each microblock of the second frame;  
code that stores the SAD value in a memory unit for each microblock of the  
second frame;  
code that calculates the sum of all the SAD values for the second frame;  
code that divides the sum by the total number of microblocks of the second  
frame.

16. The code of claim 14 that calculates a divisor value comprises  
code that selects a series of integers that is indexed from 0 through n-1;  
code that selects a complexity integer;  
code that calculates the quotient modulo n of the complexity integer;  
code that sets the divider value equal to an integer whose index in the series  
6 equals the quotient;  
7 wherein n is an integer larger than 1.

17. The code of claim 16 that selects a complexity integer comprises:  
code that sets the complexity integer near midrange between an integer A and  
3 an integer B if the second frame is an I-frame;  
4 code that adjusts the complexity integer so that the fullness of a buffer varies  
5 toward a predefined fullness level if the second frame is not an I-frame.

1           18. A system for processing digital video signals for live video  
2 applications, the system comprising:  
3           a video providing subsystem that provides video data comprising a plurality of  
4 frames;  
5           a sigmaSAD calculation subsystem that calculates a value of sigmaSAD;  
6           a divisor calculation subsystem that calculates a value of divisor.

1           19. The system of claim 18 wherein the sigmaSAD calculation subsystem  
2 comprises:  
3           a subsystem that calculates a SAD value for each microblock of a frame of the  
plurality of frames;  
4           a subsystem that stores the SAD value in a memory unit for each microblock  
of the frame;  
5           a subsystem that calculates the sum of all the SAD values for the frame;  
6           a subsystem that divides the sum by the total number of microblocks of the  
frame.

1           20. The system of claim 18 wherein the divisor calculation subsystem  
2 comprises  
3           a subsystem that selects a series of integers that is indexed from 0 through n-1;  
4           a subsystem that selects a complexity integer;  
5           a subsystem that calculates the quotient modulo n of the complexity integer;  
6           a subsystem that sets the divider value equal to an integer whose index in the  
7 series equals the quotient;  
8           wherein n is an integer larger than 1.

1           21. The subsystem of claim 20 that selects a complexity integer comprises:  
2           a subsystem that if the second frame is an I-frame, sets the complexity integer  
3 near midrange between an integer A and an integer B;  
4           a subsystem that if the second frame is not an I-frame, adjusts the complexity  
5 integer so that the fullness of a buffer varies toward a predefined fullness level.

1           22. The system of claim 18 further comprises:  
2           a quantization step calculation subsystem that sets the quantization step equal  
3 to the sum of the ratio of the value of sigmaSAD to the value of divisor, and a constant.